**Subjects included in the program, which are not taught by the instructor in the audience, but which are to be studied freely by the students:**

1. Machine-Level Representation of Programs. Program Encodings. Machine-Level Code. Data Formats. Operand Specifiers. Data Movement Instructions. Data Movement Example. Load Effective Address. Unary and Binary Operations. Shift Operations. Discussion. Special Arithmetic Operations.
2. Control. Condition Codes. Accessing the Condition Codes. Jump Instructions and Their Encodings. Translating Conditional Branches. Loops. Conditional Move Instructions. Switch Statements.
3. Procedures. Stack Frame Structure. Transferring Control. Register Usage Conventions. Procedure Example. Recursive Procedures.
4. Array Allocation and Access. Basic Principles. Pointer Arithmetic. Nested Arrays. Fixed-Size Arrays. Variable-Size Arrays.
5. Heterogeneous Data Structures. Structures. Unions. Data Alignment. Using the GDB Debugger. Out-of-Bounds Memory References and Buffer Overflow. Thwarting Buffer Overflow Attacks. x86-64: Extending IA32 to 64 Bits. Machine-Level Representations of Floating-Point Programs.
6. The Y86 Instruction Set Architecture. Programmer-Visible State. Y86 Instructions. Instruction Encoding. Y86 Exceptions. Y86 Programs. Some Y86 Instruction Details.
7. Logic Design and the Hardware Control Language HCL. Logic Gates. Combinational Circuits and HCL Boolean Expressions. Word-Level Combinational Circuits and HCL Integer Expressions. Set Membership. Memory and Clocking.
8. Sequential Y86 Implementations. Organizing Processing into Stages. SEQ Hardware Structure. SEQ Timing. SEQ Stage Implementations.
9. General Principles of Pipelining. Computational Pipelines. A Detailed Look at Pipeline Operation. Limitations of Pipelining. Pipelining a System with Feedback.
10. Pipelined Y86 Implementations. SEQ+: Rearranging the Computation Stages. Inserting Pipeline Registers. Rearranging and Relabeling Signals. Next PC Prediction. Pipeline Hazards. Avoiding Data Hazards by Stalling. Avoiding Data Hazards by Forwarding. Load/Use Data Hazards. Exception Handling. PIPE Stage Implementations. Pipeline Control Logic. Performance Analysis. Unfinished Business.